

REMARKS

This communication responds to the Office Action dated March 19, 2010. No claims are amended. No claims are canceled. Claim 45 and 46 are added. As a result, claims 1-46 are now pending in this Application.

§103 Rejection of the Claims

Claims 1-44 were rejected under 35 U.S.C. § 103(a) in view of Hughes et al. (U.S. 6,427,193, hereinafter “Hughes”), Sachs et al. (U.S. 2002/0009067, hereinafter “Sachs”) and Ghose et al. (U.S. 2002/0004842, hereinafter “Ghose”). Since a *prima facie* case of obviousness with respect to independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34, and 38 has not been properly established, this rejection is respectfully traversed.

Independent claims 1, 5, and 8:

Claim 1 recites, in pertinent part:

a load/store unit that includes a retry logic that is to retry access to a memory resource operatively coupled to the apparatus *after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource* by the load/store unit; and

a congestion detection logic *to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments* in response to access requests to the memory resource.

Similar elements are recited in independent claims 5 and 8. Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the above-quoted elements recited in claim 1.

The Office Action states at p. 2, paragraph 4, lines 1-4, that col. 39, lines 20-32 of Hughes teaches the claimed elements, namely, “a load/store unit that includes a retry logic that is to retry access to a memory resource *after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource* by the load/store unit.” The

Office Action further states at p. 21, paragraph 55, Response to Arguments, that “[w]hile the Sachs and Ghose references may not teach receiving negative acknowledgements from a memory resource, the Hughes teaches receiving a NACK from the cache memory, as described above in col. 39, lines 20-32.” Applicant respectfully disagrees.

Hughes discusses a load/store unit that is configured to back off from retrying to access a cache line for which ownership was lost for a given time interval (“backoff time”). The load/store unit in Hughes automatically resumes attempting to reestablish the ownership for the cache line and to access the cache line after expiration of the given time interval (“backoff time”). This is described in Hughes, as follows:

On the other hand, processor 10 loses sufficient ownership to complete a store memory operation if a cache line accessed by the store is previously in a state other than invalid or shared and the cache line is changed to invalid or shared in response to a snoop hit. In response to losing sufficient ownership, load/store unit 26 is configured to signal bus interface unit 37 to backoff (via a backoff signal on backoff line 336) and to increase the initial backoff time. The backoff time is increased each time the ownership is gained and then lost before the affected memory operation can be completed. Eventually, the memory operation may be completed (after the other processor successfully completes its memory operation) and the backoff time may be reset to its initial value. *The term “backoff time” refers to a time interval during which processors are configured to inhibit attempting to reestablish ownership of a cache line for which ownership was lost via a snoop operation.* It is noted that load/store unit 26 may be configured to perform the backoff internally (e.g. by not attempting to transmit commands to bus interface unit 37 for transmittal on the bus).

Hughes at col. 39, lines 16-35 (emphasis added).

While processor 1 is backed off, processor 2 attempts to reestablish ownership of cache line A2 (reference numeral 374). Again, the operation may be a read with modify intent. Processor 1 loses ownership of cache line A1 in response to snooping processor 2's operation. Processor 2 then has exclusive ownership of both cache lines A1 and A2. However, prior to processor 2 completing the store operation, *processor 1's backoff interval expires and processor 1 attempts to reestablish ownership of cache line A1*

(reference numeral 376). Processor 1 snoops the operation and loses ownership of cache line A1. Additionally, processor 1 enters a backoff interval of the initial length as well.

Hughes at col. 42, lines 17-43 (emphasis added); *see also* col. 42, lines 34-36.

Although, as quoted above, the load/store unit in Hughes signals the bus interface unit 37 to backoff from further attempting the cache line for which ownership was lost, Hughes does not teach or suggest that the load/store unit in Hughes receives a NACK from a memory resource including the cache line, as asserted in the Office Action. Furthermore, as noted above, the load/store unit in Hughes automatically resumes attempting to reestablish the ownership for the cache line after expiration of the backoff time. Given these teachings, Hughes fails to show “a load/store unit that includes a retry logic that is to retry access to a memory resource operatively coupled to the apparatus *after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource* by the load/store unit,” as recited in claim 1.

Applicant is unable to find any such teaching within the bounds of Hughes, Sachs or Ghose, alone or in combination.

In addition, as admitted in the Office Action at p. 2, paragraph 4, line 5, Hughes fails to show “a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource,” as recited in claim 1. The Office Action states at p. 2, third last line through p. 3, line 5, that the combination of Sachs, Ghose and Hughes discloses these elements recited in claim 1. Applicant respectfully disagrees.

Sachs discusses adapting to congestion in a network between a user equipment and a radio base station. *See* Sachs at paragraphs [0028], [0038] and [0044]. Under Sachs’ approach, the negative acknowledgement is returned from the network, and not from a memory resource, as required by claims 1-44. In particular, Sachs teaches that “if a negative acknowledgment as an indication of congestion is returned from the network, the user equipment uses a longer “Subsequent Backoff Delay 2” to ease the load on the [network] channel.” Sachs at paragraph [0052], lines 13-18. Furthermore, Sachs does not describe that the congestion in the network is caused by multiple retry requests to access the memory resource. Finally, as admitted in the Office Action at p. 3, lines 1-2, Sachs fails to teach that it takes more than one consecutive negative acknowledgements to indicate the network is congested. Therefore, Sachs fails to show

“a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource,” as recited in claim 1.

Ghose discusses coping with congestion in a network. *See* Ghose, paragraph [0117], lines 15-16. In particular, Ghose discusses “network congestion as evidenced by ... the generation of a predetermined number of NACKs ... during a predetermined time interval.” Ghose, paragraph [0117], last six lines. That is, Ghose deals with the congestion in the network, and not in a memory resource. Furthermore, Ghose does not describe that the congestion in the network is caused by multiple retry requests to access the memory resource. Finally, although Ghose uses a plurality of NACKs as an indication of the network congestion, Ghose fails to teach that the plurality of NACKs are consecutive, as required by claims 1-44.

The Office Action further states at p. 3, lines 4-5, that “Hughes teaches an NACK from the memory resource, so the combination of Hughes with Sachs teaches this limitation.” As noted above, however, Hughes does not teach or suggest that the load/store unit in Hughes receives the NACK from the memory resource, as asserted in the Office Action. Therefore, the combination of Sachs, Ghose and Hughes fails to show “a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource,” as recited in claim 1. Applicant is unable to find any such teaching within the bounds of Sachs, Ghose or Hughes, alone or in combination.

The arguments in support of the patentability of claim 1 similarly apply to independent claims 5 and 8, which each recite similar limitations.

Independent claims 12, 17, 22, 31, and 38:

Amended independent claim 12 recites, in pertinent part:

a congestion detection logic to detect congestion of access to the data from the cache memory based on receipt from the cache memory of a consecutive number of negative acknowledgments in response to the access requests.

For the same reasons as have been noted with respect to independent claims 1, 5, and 8, Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the elements as recited in independent claim 12. The arguments in support of the patentability of claim 12 similarly apply to independent claims 17, 22, 31, and 38, which each recite similar limitations.

Independent claims 27 and 34:

Independent claim 27 recites, in pertinent part:

receiving, by the first processor, a positive acknowledgment or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests; and

detecting congestion of the data in the memory based on receipt, by the first processor, of a consecutive number of negative acknowledgments from the second processor that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment from the second processor.

For reasons similar to those noted with respect to independent claims 1, 5, and 8, Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the above-quoted elements recited in independent claim 27. In particular, combination of the cited documents does not show “receiving, by the first processor, a positive acknowledgment or a negative acknowledgment *from a second processor* that is associated with the memory” or “detecting congestion of the data in the memory based on receipt, by the first processor, of a consecutive number of negative acknowledgments *from the second processor* that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment from the second processor,” as recited in independent claim 27. The arguments in support of the patentability of claim 27 similarly apply to independent claim 34, which recites similar limitations.

For at least the reasons stated above, Applicant respectfully submits that the Office Action fails to show a prima facie case of obviousness with respect to independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38, and that these claims are in condition for allowance. Therefore,

reconsideration and allowance of independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38 are respectfully requested.

Claims 2-4, 6, 7, 9-11, 13-16, 18-21, 23-26, 28-30, 32, 33, 35-37, 39 and 40 are submitted to be allowable as depending from their respective independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38, which are submitted to be allowable.

In addition, regarding claims 14, 19, and 24, neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests "the second processor is to transmit a negative acknowledgment back to the first processor through the hub controller if the memory resource is not accessible, the second processor to transmit a positive acknowledgment back to the first processor through the hub controller if the memory resource is accessible," as recited in claims 14, 19, and 24.

The Office Action states at pp. 9-10, paragraph 21, that FIG. 25 and col. 43, lines 15-25 of Hughes disclose these claimed elements. Applicant respectfully disagrees.

Hughes discusses using "bus bridge 202" coupled to two processors ("processor 10" and "processor 10a"). *See* Hughes at FIG. 25. Even if all requests between the processor 10 and the processor 10a are channeled through the bus bridge 202, as asserted in the Office Action at p. 10, lines 1-3, Hughes does not teach or suggest that the processor 10 attempts to access the "L2 cache 228a" that is locally coupled to the processor 10a. Furthermore, Hughes does not teach or suggest that the processor 10a transmits a positive acknowledgement or a negative acknowledgement to the processor 10 in response to receipt of the access request to the L2 cache 228a, if any, from the processor 10. Applicant is unable to find any such teaching within the bounds of Hughes, Sachs or Ghose, alone or in combination.

For at least the reasons stated above, reconsideration and allowance of claims 2-4, 6, 7, 9-11, 13-16, 18-21, 23-26, 28-30, 32, 33, 35-37, 39 and 40 are respectfully requested.

New Claims

Claims 45 and 46 are new. Support for the new claims may be found in the specification as originally filed, for example, at FIG. 1 and original claims 22 & 23. Thus, Applicant believes that no new matter has been introduced in the added claims. Independent claim 45 recites elements similar to those of independent claim 12. Therefore, Applicant respectfully submits

that independent claim 45 and its dependent claim 46 are allowable for at least the same reasons as independent claim 12. Consideration and allowance of claims 45 and 46 are respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6909 to facilitate prosecution of this application.

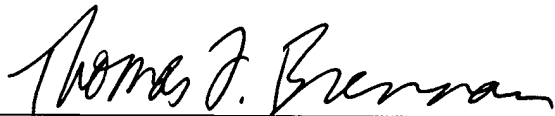
If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No.19-0743.

Respectfully submitted,

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Date August 19, 2010

By



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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 19th day of August, 2010.

Name

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